An 80W AlGaN/GaN Heterojunction FET with a Field-Modulating Plate

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Abstract — **An AlGaN/GaN heterojunction FET with a field-modulating plate (FP) has been fabricated on a SiC substrate. The gate breakdown voltage (BV_{gd}) was improved from 50V to 160V by introducing an FP electrode. The highest BV_{gd} was obtained with an FP length of 1.0 μm. A 4mm-wide unit-cell FET exhibited 32.5W (8.1W/mm) output power, 62% power-added efficiency, and 12.4 dB linear gain at a drain bias of 41V. The linear gain decreased with increasing the FP length, but the difference in the linear gain among FETs with various FP lengths decreased with increasing the drain bias. To the best of our knowledge, a power density of 8.1W/mm is the highest for GaN based FETs with over 1mm gate width. For a 24mm-wide 6-cell FET, an output power of 80.0W (3.3W/mm) was obtained with a linear gain of 8.5dB and a power-added efficiency of 42% at a drain bias of 31V.**

I. Introduction

GaN technology for high power microwave devices has shown a steady progress over the last several years. Small periphery devices, made up of only one or two gate fingers, have demonstrated high power density, including 11.7W/mm for a 100μm-wide device [1] and 10.3W/mm for a 300μm-wide device [2]. The power density, however, generally degraded as the gate width increased to more than 1mm, where a power density of 5.7W/mm was reported as a record with a gate width of 4mm [3]. For larger periphery devices, a total output power of 102W (4.3W/mm) [4] and 113W (3.5W) [5] has been reported. In order to achieve higher power density for large periphery devices, higher breakdown voltage and high RF drain current are essential together with a thermal management and a low-loss impedance matching circuit design.

In this work, a field-modulating plate (FP) structure [6] is applied for achieving a high breakdown voltage and suppressing current collapse. The developed FET with an FP electrode (FP-FET) demonstrated a record output power density for multi-finger unit-cell FETs. For a 6-cell single-chip FET, a total output power of 80W was obtained.

II. Device Structure and Fabrication

The AlGaN/GaN heterojunction FET developed in this study is schematically shown in Fig.1. An undoped $Al_{0.25}Ga_{0.75}N$/GaN heterostructure was grown on a SiC substrate. Ti/Al ohmic electrodes were fabricated by lift-off technique and alloyed using rapid thermal annealing at 650°C. Device isolation was achieved by nitrogen ion implantation. SiN was deposited using plasma-enhanced chemical vapor deposition as a surface passivation film. Ni/Au was used as a gate electrode material. The gate length was 1.0μm. The eaves of the gate electrode overhang on the SiN film toward the drain electrode and function as FP electrodes. The FP length (L_{FP}) was varied from 0.5μm to 2.0μm, whereas the gate-drain spacing was fixed to 2.5μm. A standard Au-plated air-bridge process was used to fabricate multi-finger FETs.

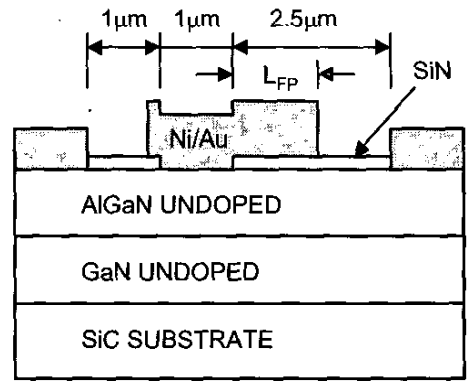

Fig.1 Schematic of fabricated AlGaN/GaN heterojunction FET with a field-modulating plate.

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III. Device Characteristics

A. DC Characteristics

DC characteristics were measured for a 50μm-wide FET. Fig.2 shows dependence of the maximum drain current (I_{max}) and the gate-drain breakdown voltage (BV_{gd}) defined at a gate current of -1mA/mm on L_{FP}. I_{max}, defined at a drain voltage (V_{ds}) of 10V and a gate voltage of +1V, was 0.8A/mm for both FP-FETs and FETs without FP (conventional FETs), and was independent of L_{FP}. Introducing the FP electrode improved BV_{gd} from 50V to 160V. An appreciable increase in BV_{gd} was seen with increasing L_{FP} up to L_{FP}=1.0μm since the FP electrode reduced the electric field strength under the gate near the drain side. On the other hand, BV_{gd} gradually reduced for the FETs with L_{FP} longer than 1.5μm since the electric field at the FP edge increased with decreasing the spacing between the FP edge and the drain edge. Thus, it turned out that L_{FP} of around 1.0μm is the best choice to achieve reasonable high-voltage power operation.

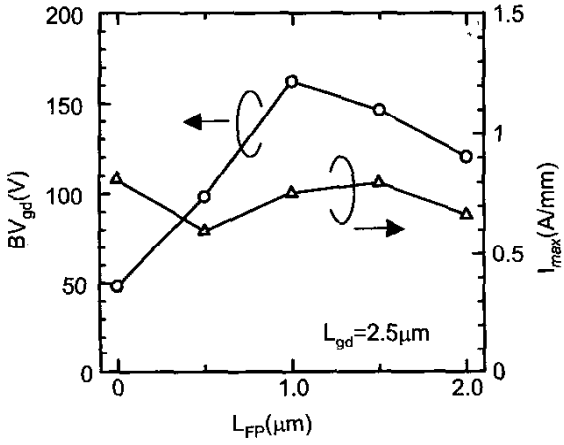

Fig.2 Dependence of maximum drain current and gate breakdown voltage dependence on the FP length.

B. Current Collapse

Fig.3 shows the drain I-V characteristics measured by a curve-tracer. The degree of current collapse was evaluated as the I_{max} difference observed between V_{ds} sweeps up to 10 and 80V. The FP-FET with L_{FP}=1.0μm exhibited no current collapse by a V_{ds} sweep up to 80V. On the other hand, I_{max} decreased by about 20% for the conventional FET by the same V_{ds} sweep These results indicate that the FP structure is effective for suppressing current collapse caused by the surface trapped charge, and enables large drain current swing during large signal RF operation.

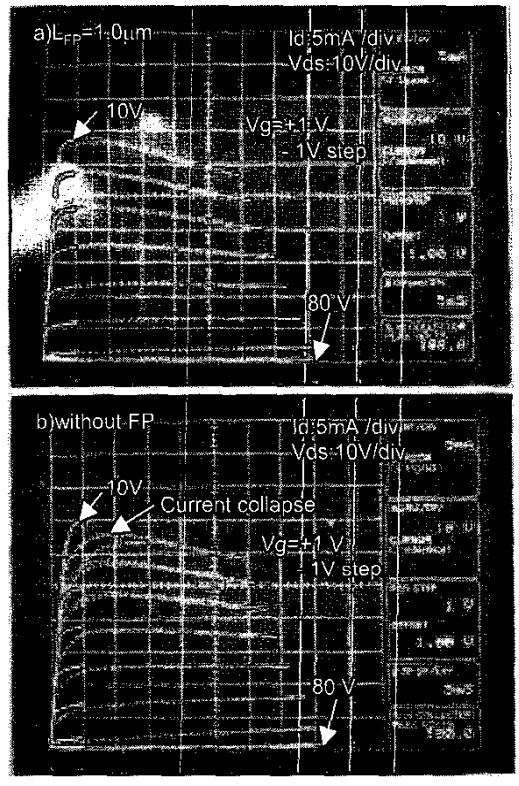

Fig.3 Drain I-V characteristics for a FP-FET (a) and a conventional FET(b) measured by a curve-tracer.

C. On-Wafer Power Measurement

On-wafer load-pull power measurements were performed at 2GHz for a 1mm-wide FET. Fig.4 shows the saturated output power (P_{sat}) for an FP-FET and that for a conventional FET plotted as a function of the drain bias (V_{dd}). The FP-FET exhibited an almost linear increase in P_{sat} with increasing V_{dd}, which is consistent with the theoretical class-A limit supposing I_{max}=0.8A/mm. The insufficient increase rate of P_{sat} observed for the conventional FET is due to the effect of current collapse.

D. Packaged Device Power Measurement

A unit-cell FP-FET, made up with 10 gate fingers, was packaged into a ceramic carrier. The FP-FET had a total gate width (W_g) of 4mm with a unit gate width of 400μm. Figs.5(a) and (b) show P_{sat} and linear gain as a function of V_{dd} for FP-FETs with various L_{FP}. The FP-FET with L_{FP}=1.0μm exhibited a linear increase in P_{sat} up to 41V. The FP-FET with L_{FP}=0.5μm exhibited almost the same output power density with that for L_{FP}=1.0μm. The FP-

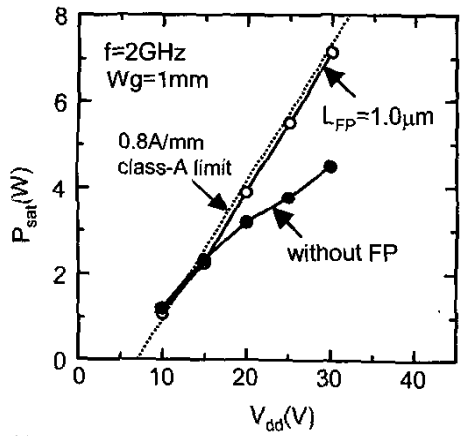

Fig.4 Dependence of the saturated output power on the drain bias for a 1mm-wide FP-FET and a conventional FET.

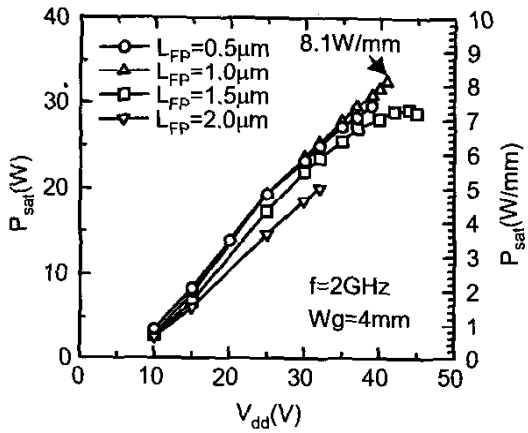

Fig.5(a) Dependence of the saturated output power on the drain bias for 4mm-wide FP-FETs with various FP lengths.

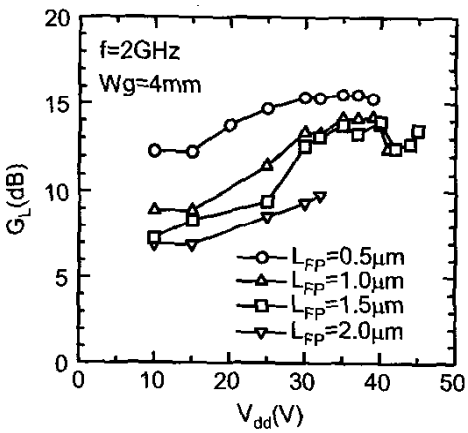

Fig.5(b) Dependence of linear gain on the drain bias for 4mm-wide FP-FETs with various FP lengths.

FET with L_{FP}=1.5μm, however, exhibited saturation of P_{sat} at V_{dd}>40V because the drain voltage swing was limited by gate breakdown. The linear gain (G_L) tends to decrease with increasing L_{FP}, but the difference in linear gain becomes smaller with the increase in V_{dd}. For example, the difference in G_L between L_{FP}=0.5μm and L_{FP}=1.0μm was 3.3dB at V_{dd}=10V, and was 2.0dB at V_{dd}=30V.

Fig.6 shows output power (P_{out}), G_L and PAE of the FP-FET with L_{FP}=1.0μm as a function of input power (P_{in}) at V_{dd}=41V. P_{sat} of 32.5W (8.1W/mm) was obtained with G_L of 12.4dB and PAE of 62%. Fig.7 shows P_{out}, G_L and PAE for a 5-cell FP-FET (W_g=20mm) as a function of P_{in} at V_{dd}=32V. P_{sat} of 75.2W (3.8W/mm) was obtained

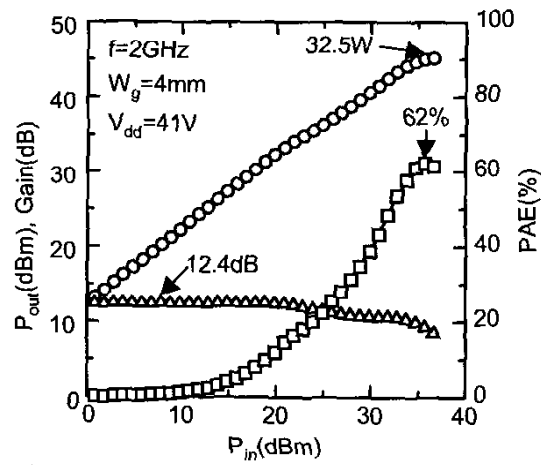

Fig.6 Output power, linear gain and power-added efficiency for a 4mm-wide FP-FET with FP length of 1.0μm as a function of input power.

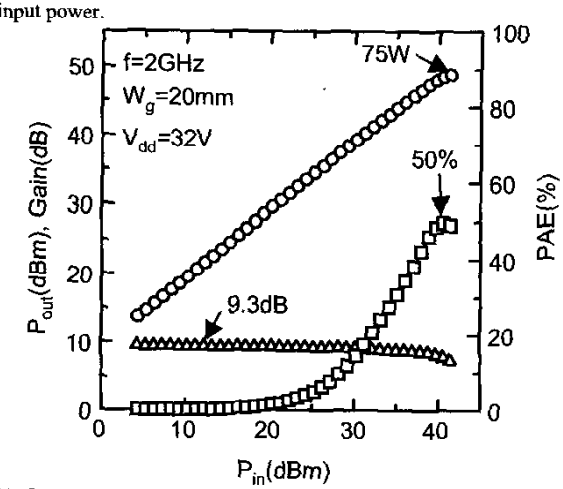

Fig.7 Output power, linear gain and power-added efficiency for a 20mm-wide FP-FET as a function of input power.

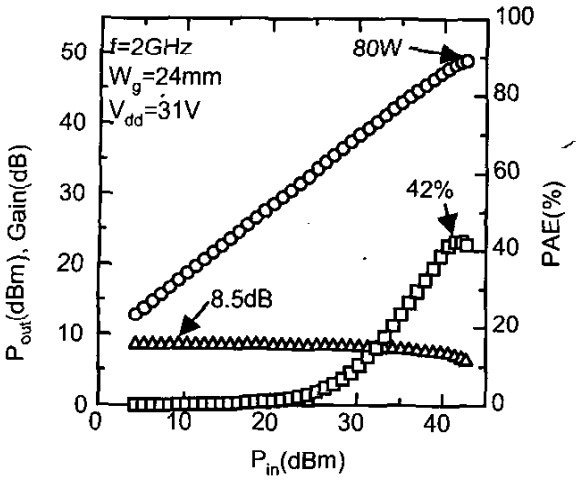

Fig.8 Output power, linear gain and power-added efficiency for a 24mm-wide FP-FET as a function of input power.

with G_L of 9.3dB and PAE of 50%. A 6-cell FP-FET (W_g=24mm) demonstrated P_{sat} of 80.0W (3.3W/mm), G_L of 8.5dB and PAE of 42% at V_{dd}=31V as shown in Fig.8. The reduction in output power density and G_L observed for the multi-cell FET results from the thermal effect and the increase of circuit losses with increasing impedance transform ratio.

Results of power measurements for the FP-FETs developed in this work are summarized in Fig.9, together with the previous results for GaN FETs[1-4]. To the best of our knowledge, a power density of 8.1W/mm is the record among GaN-based FETs with more than 1mm gate width.

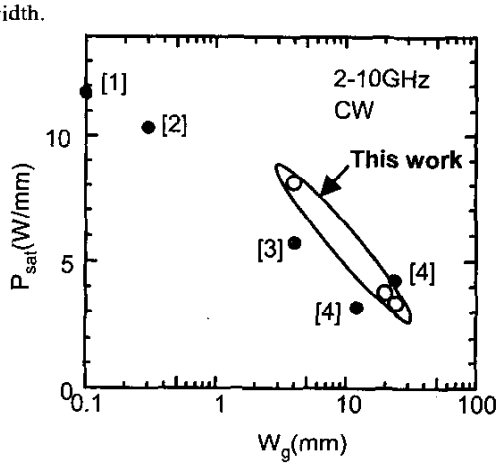

Fig.9 Power performance of the FP-FETs developed in this work and that of previously reported GaN FETs.

IV. Conclusion

An AlGaN/GaN heterojunction FET with a field-modulating plate has been fabricated on a SiC substrate. The FP structure enables both achieving a high breakdown voltage and suppressing current collapse. It turned out that the FP length around 1.0μm is the best choice to achieve reasonable high-voltage power operation. A 4mm-wide FP-FET exhibited a record output power density of 8.1W/mm among GaN-based FETs with more than 1mm gate width. A 24mm-wide FP-FET demonstrated a total output power of 80W at a drain bias of 31V. These results indicate that the AlGaN/GaN FET with a field-modulating plate is promising as a high-voltage operation power device.

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